

GENERAL DYNAMICS | CONVAIR

PHASE I FINAL REPORT

↗  
SIMULATION  
OF SELECTED DISCRETE NETWORKS

VOLUME THREE

SATURN I-C  
ENGINE CUTOFF SYSTEM MODEL  
CONTRACT NAS8-20016

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Prepared by

GENERAL DYNAMICS/CONVAIR  
A Division of General Dynamics Corporation  
Huntsville, Alabama

for

George C. Marshall Space Flight Center  
Huntsville, Alabama

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## INTRODUCTION

The Discrete Network Simulation (DNS) system is based on simulation and analysis techniques developed for the Atlas Weapon System under government and corporate sponsorship. The total technique as applied to the Atlas Weapon System was called FASTI, Fast Access to System Technical Information. This study uses the Discrete Network Simulation portion with a modified version of the documentation and retrieval process. Digital computer programs are used to simulate discrete networks in less than real time. These programs were developed by GD/A and then incorporated into the FASTI system.

The prime purpose of Discrete Network Simulation methodology is to provide a set of analytical tools capable of conducting thorough, accurate and rapid analysis of complex systems. The methodology consists basically of:

- A system network model.

- A set of computer programs which will operate and activate the model.

These programs provide a realistic analysis and prediction of system performance before or after the hardware system is constructed. It is another form of testing; the results are as valid as those obtained by the more common hardware test procedures.

The Discrete Network Simulator (DNS) chronologically simulates events occurring due to the interactions among elements in a system network. Each "event," a Boolean change of state, is the result of a logical cause and effect relationship among elements in the system. The system modeled for the simulation may be a switching circuit, man/machine interaction, or any network where the component or subcomponent interrelations may be defined logically.

Convair is conducting a study under NASA Contract NAS8-20016, which applies the Discrete Network Simulation techniques to the Saturn S1C Engine Cutoff System networks. This report summarizes the results of Phase I and consists of three (3) volumes.

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Volume One describes the methodology for constructing a DNS model.

Volume Two describes the DNS computer programs to the "Programmer." It is the "Users Reference Manual" for DNS.

Volume Three summarizes the study of the SIC Engine Cutoff System. The DNS Model and examples of the system simulation are described.

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## VOLUME THREE INTRODUCTION

In Volume I of this report the methodology and guidelines for building a Discrete Network Simulation (DNS) model are described.

Volume II of this report is the Users Reference Manual for the Computer programs that simulate in terms of real time a discrete system described by the logic model. These two techniques were applied to a group of Saturn I-C Stage and GSE networks to develop a model of the Engine Cutoff System.

Volume III defines the model and demonstrates how this model with the programs simulate the hardware system. The output from the DNS programs can be varied to suit the application. Examples of the different output modes are explained.

The initial production models of a new stage are subject to a series of engineering changes prior to the first operational vehicle. The value of an analytical tool, such as DNS, is dependent upon how conveniently and economically the model can reflect the latest hardware configuration. An engineering change was incorporated in the DNS model after it had been completed and several simulation runs conducted. The results of this engineering change incorporation is summarized.

One application for the DNS model is to analyze how the failure of critical components would affect the system operation. To demonstrate this application, the DNS model was run after programming into it failures of selected components at specified times in the normal operation. The results of these simulations are condensed and summarized in this report.

The DNS programs, combined with a logic model of the hardware system, provide an analytical tool that can be applied to many different specific applications. This report gives examples of some of the possible applications of Discrete Network Simulation.



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## 1/DISCRETE NETWORK SIMULATION

### 1.1 SYSTEM MODEL

Authorization to start work on this contract was received by Convair on 6 April 1965. Concurrent with go-ahead, the Vehicles Systems Checkout Division reviewed their schedules and recommended that the analytical portion of this contract be applied to the SIC Electrical Networks rather than the SIA Instrument Unit, as originally planned. A preliminary analysis of five recommended electrical network sub-systems was made to determine which combination of systems would allow an analysis to be made that would be comparable to the task originally proposed. As a result of the analysis, it was agreed that Discrete Network Simulation would be applied to the SIC Engine Cutoff System. The Engine Cutoff System and related ESE was sufficiently complex to demonstrate the capability of the technique and was not too large for the time allotted, although larger than the model originally proposed.

The SIC Engine Cutoff System consists of many inter-related branch circuits. Each branch circuit consists of several components connected in series interdispersed with other parallel circuits. The objective of writing the logic equations is to subsequently allow the computer programs to simulate the real time action of these components acting as a system and then to inject into this simulation component malfunctions and observe their effect upon the system.

Table 3-I lists the schematics that were used to write the equations for the DNS model. In some cases only parts of the networks on a given sheet were included. When all the equations had been written, over 2,500 variables had been defined that included over 1,100 components, signal sources, or monitoring points. The total distribution of the type of equipment included in the model is shown in Table 3-II.

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TABLE 3-1A  
SIC NETWORKS IN DNS MODEL  
DRAWING 60B55701  
SIC STAGE ELECTRICAL SCHEMATICS

Sheet

12	Batteries and Changeover Regulation
24	Lox Interconnect System
25	Engine No. 1 Ignition System
26	Engine No. 2 Ignition System
27	Engine No. 3 Ignition System
28	Engine No. 4 Ignition System
29	Engine No. 5 Ignition System
30	Inboard Engine Cutoff System
31	Outboard Engine Cutoff System
32	Outboard Engine Cutoff System
33	Cutoff Circuitry Engine No. 1
34	Cutoff Circuitry Engine No. 2
35	Cutoff Circuitry Engine No. 3
36	Cutoff Circuitry Engine No. 4
37	Cutoff Circuitry Engine No. 5
38	Lox Prevalves
39	Fuel Prevalves
40	Fuel Prevalve Position Indication
41	Lox Prevalve Position Indication
42	Stage Sequencing Switch Selector
43	Stage Sequencing Switch Selector

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TABLE 3-1B  
DRAWING 65B32000  
ADVANCED ELECTRICAL/MECHANICAL SCHEMATICS

## Sheet

178	Terminal Countdown Sequencer Unit 384
287	GSE Stage DC Power Supply No. 1
292	GSE Stage DC Power Supply No. 2
445	Upper Stage Electrical Networks Substitute
449B	Switch Selector Control
524A	Michoud Only
568	All Prevalves Control & Monitor
568A	All Prevalves Control & Monitor
569	All Prevalves Control & Monitor
569A	All Prevalves Control & Monitor
570	All Prevalves Control & Monitor
570A	All Prevalves Control & Monitor
572	Lox Interconnect Valves
574	Lox Interconnect Valves
575	Main Lox Valves
577	Main Fuel Valves
605	Fuel Pre-pressurization
609	Ignition Circuitry
614	Ignition Circuitry
615	Rough Combustion
616	Engine Malfunction
617	Engine Malfunction
618	Engine Malfunction
618A	Engine Malfunction
619	Thrust OK
619A	Thrust OK
620	Thrust OK
621	Engine Cutoff Circuits
622	Engine Cutoff Circuit Simulated Static Firing
624	Engine Cutoff Circuits
624A	Launch Commit, Simulated Static Firing
643D	Launch Commit, Simulated Flight
643F	Engine Cutoff Circuits Simulated Flight

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TABLE 3-II  
DISTRIBUTION OF VARIABLES IN DNS MODEL OF  
SIC ENGINE CUTOFF SYSTEM

<u>Variable</u>	<u>Quantity</u>
Relay Contact	262
Relay Coils	169
Diodes	162
Miscellaneous	128
Signal sources	
Lights	70
Switches	59
Discrete Inputs	55
Timers	30
Power Buses	24
Discrete Output	23
Solenoids	21
	<hr/>
	1,103
Nodes	246
Legs	776
Dummies	383
	<hr/>
	1,405
TOTAL	2,508

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### 1.2 COMPONENT ACTIVATION TIME

In addition to writing logic equations for the network to be simulated, the activation time for the active variable in the system must be specified. The simulation program requires both activation (pickup) and de-activation (dropout) to be specified. Since these are not absolute but represent the average of many identical components, the program allows a range of times to be specified. These are referred to as minimum, average, and maximum. Thus, there are six times supplied for each variable. The set to be used with a single simulation must be listed with the input data.

The timing information for the relays was supplied by MSFC. These times were obtained from the manufacturer's specifications. The activation times for the propulsion system valve were obtained from the system operating description. The information for the timers was detailed on the schematics. It should be noted that many variables in the equation such as connector, nodes, and legs are given zero times to signify instantaneous reaction. The significant time parameters used in the model are listed in Table 3-III.

TABLE 3-III  
COMPONENT ACTIVATION TIMES

RELAYS	PICKUP			DROPOUT		
	MIN.	OVER	MAX.	MIN.	AVER.	MAX.
Babcock Model						
BRJ26K1AX6A-1	4	5	6	4	5	6
BR7X-300-D8-26V	5	6	7	5	6	7
United States Relay Model						
USSH35EKHXI	13	15	17	5	6	7
PREVALVES	450	500	550	450	500	550
MAIN FUEL VALVE	1,100	1,200	1,300	1,100	1,200	1,300
MAIN LOX VALVE	450	500	550	450	500	550

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### 1.3 DNS DOWN TRANSLATION AND CULLING PROGRAM

This program has been developed by Convair to increase the capability and flexibility of the DNS Program in two ways. In the first DNS Computer Programs, each variable or component in the equation had to be described with a coded symbol made up of less than six characters. In many cases this required a secondary coding of each component in a more condensed form than would normally appear on a schematic diagram. This made the verification and check-out of the simulation more difficult. The new program allows each variable to be described as it appears on the schematic, using as many as 24 characters. The Down Translation and Culling Program (DT&C) assigns to each variable an arbitrary three-letter code. This three-letter symbol is subsequently used in the remaining DNS Programs, including the simulation.

1.3.1 When the logic equations are written the first time, every identifiable element in the circuit is included in the equation. Many of these elements, such as connectors and terminals, are inactive in the sense that during the normal operation of the system they do not change state at any time. It is desirable to include these inactive variables in the equations for the sake of completeness and to include the ability to investigate the effect of their failure during subsequent analysis. The culling portion of this program strips the logic equations of those elements which have been defined as "Inactive." This classification is included with the timing information for each element. Eliminating these variables reduces the computer running time for the simulation program.

Figure 3-1 shows a page of the DT&C printout of the logic model of the Engine Cutoff System. This printout is a direct copy of the information key punched during the model preparation phase, which indicates the time parameters for the variables in the model. The only additional information present on this printout is the arbitrary assignment of the three-letter variable code names to each of the engineering designations for the variables. The format for this printout is the same as that for the punch cards and is explained in Volume I.

1.3.2 The second printout from the DT&C Program is shown in Figure 3-2. One asterisk indicates the original equation as it was punched on the card. The variable name takes up to the first 24 spaces on the card. Following the equal sign is the remainder of the logic describing that variable. If this equation cannot be described on one card, additional cards are used. There is no limit to the number of cards that can be used. On the right side of the page is the sheet number of the schematic from which this equation was written and an arbitrary number that indicates that this is the "X" equation that was written from that sheet by the analyst. The column at the extreme right indicates the card number in the equation.







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The line with two asterisks is the culled equation. In the culled equation, as previously defined, all variables that were classified as Inactive on the time-card are removed from the equation. The third line containing three asterisks designates the translated equation. The DT&C Program has taken the culled equation and replaced the engineering designation by the three-letter variable. It is possible to have a line containing four asterisks. This is an "error flag" if an equation has a variable name included for which there is no time-card, and consequently, no code name assigned. The printout cannot be completed and the four-asterisk flag is printed.

1.3.3 Appendix A is the DT&C printout of the completed model of the SLC Engine Cutoff System. This model contains approximately 2,510 variables. This printout is not the primary output of the DT&C Program. The activation time information, the equations, and a dictionary of the engineering names versus code names is placed on the output tape. This tape is the data output from the DT&C Program and provides the input data to the DNS Preprocessor, which is the next phase in the DNS Program.

### 1.4 DNS PREPROCESSOR PROGRAM

The Preprocessor Program utilizes the output of the Down Translation and Culling Program to create a binary tape, which is the input to the Simulation Program. The tape represents the source data describing the model in the format required by the Simulation Program. It also produces a listing of the logic equations and timing information that may be checked against the original schematic diagrams. Self-checking diagnostic features are built into the program to insure that every variable in the right hand side of any equation also appears on the left hand side of an equation and is thus defined. It also checks that activation time information has been supplied for each variable. These error flags are included in the printout of this program. Detailed information about the Preprocessor Program is contained in the User Reference Manual, Volume II of this report.

Figure 3.3 is a composite sample of the three types of printout produced by the Preprocessor Program. These printouts are mainly for reference use during the model building process and have no direct analytical value. The primary output of the Preprocessor Program is the binary tape which is the input to the Simulator Program. The first portion of the Preprocessor printout is identical to the component time-cards in the DT&C Program with the exception that the engineering names have been deleted. The second printout lists the logic equations that make up the system model using only the computer coded symbols and the reference information. For future use with the Simulator Program, the Preprocessor tape and printout also contains the reference dictionary of computer code names versus engineering names for each variable listed in the DT&C. Appendix B is the printout of the Preprocessor Program for the total model of the Engine Cutoff System.

PREPROCESSOR	SIC ENGINE CUTOFF SYSTEM	A.R. STØNE	0000
AFM	S OS OS 0 S OS OS 0	AD X X0	AD X X0
AFN	S OS OS 0 S OS OS 0	AD X X0	AD X X0
AFØ	S OS OS 0 S OS OS 0	AD X X0	AD X X0
AFP	S OS OS 0 S OS OS 0	AD X X0	AD X X0
AFQ	S OS OS 0 S OS OS 0	AD X X0	AD X X0
AFR	S OS OS 0 S OS OS 0	AD X X0	AD X X0
AFS	S OS OS 0 S OS OS 0	AD X X0	AD X X0
AFT	S OS OS 0 S OS OS 0	AD X X0	AD X X0
AFU	S OS OS 0 S OS OS 0	AD X X0	AD X X0
AFV	S OS OS 0 S OS OS 0	AD X X0	AD X X0
AFW	S OS OS 0 S OS OS 0	AD X X0	AD X X0
AFX	S OS OS 0 S OS OS 0	AD X X0	AD X X0
AFY	S OS OS 0 S OS OS 0	AD X X0	AD X X0
AVB = BLC * BAF		618 20 1	
AVP = / BMØ * AGK * / AUK		617 39 1	
AVQ = / BMG * AGK * / AUJ		617 40 1	
AVR = / BQZ * AFU * / ASG		617 41 1	
AVS = / BJP * AGZ * / AMG		617 42 1	
AVT = BLY * BAF		617 43 1	
AVU = / BMK * AGN * / AUT		616 24 1	
AVV = / BML * AGN * / AUS		616 25 1	
AVW = / BRF * AFW * / ASØ		616 26 1	
AVX = / BJK * AHA * / AMJ		616 27 1	
AVY = / BLW * BAF		616 28 1	
AVZ = / HMM * AGM * / AUQ		616 14 1	
AWA = / BMN * AGM * / AUP		616 15 1	
AWB = / BRB * AFV * / ASJ		616 16 1	
AWC = / BJM * AHB * / AMM		616 17 1	
AWD = BLX * BAF		616 18 1	
AWE = BAK		624 58 1	
AWF = BAK		624 59 1	
BTZ	LITE308AIDS90R		
BUA	LITE308AIDS91R		
BUB	LITE308AIDS92R		
BUC	LITE308AIDS94R		
BUD	LITE308AIDS95R		
BUE	LITE308AIDS96R		
BUF	LITE308AIDS97R		
BUG	LITE400AIDS123R		
BUH	LITE400AIDS135R		
BUI	LITE400AIDS139R		
BUJ	LITE400AIDS140R		
BUK	LITE400AIDS166R		
BUL	LITE400AIDS170R		
BUM	LITE400AIDS171R		
BUN	LITE400AIDS197R		
BUØ	LITE400AIDS201R		
BUP	LITE400AIDS202R		
BUQ	LITE400AIDS228R		
BUR	LITE400AIDS232R		

EXAMPLE OF THE THREE TYPES OF PRINTOUT OF THE PREPROCESSOR PROGRAM

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### 1.5 DISCRETE NETWORK SIMULATION PROGRAM

The input to this program is the binary tape produced by the DNS Preprocessor Program and a set of control cards used to establish initial condition of selected variables in the system. See Volume II, Users Reference Manual, for an explanation and proper use of the control cards for the Simulation Program. Figure 3-4 is a typical first page of the printout from the Simulation Program. The Simulation Program will be described in reference to Figure 3-4. For convenience of interpretation, the function of the more common control cards used with the Simulation Program will be repeated from Volume II.

**1.5.1 BINARY OUTPUT.** The Simulation Program has two different modes of operation. The Preprocessor tape and the internal Simulator Program operates on all data in binary format. The output data must be converted back to binary coded decimal format for printout. On the IBM 7094 computer all output data is placed on magnetic tape and printed offline on the IBM 1401. In the simulation process using the basic mode of operation, the simulation analysis is performed and the results are translated from the computer code to engineering names. This data is then translated into Binary Code Decimal (BCD) and recorded on tape for subsequent printing. This mode of operation requires the maximum amount of computer memory for a given size model. If the binary output control card is included with the input data, then the simulation run, and all the data associated with it, is recorded on a tape in binary format. At the end of the simulation process this tape is rewound, played back into the computer, and the binary data is translated to engineering terms converted to BCD and recorded on the output tape.

**1.5.2 LOGICAL MODE.** The Logical Mode card establishes the program in the proper configuration to perform the simulation. Immediately to the right of the logical mode are two numbers, "02" and "05." These numbers specify which of the six possible activation times listed in the preprocessor will be used for this simulation. The "01" to "03" refers to the pickup times and the "04" to "06" refers to the dropout. As it explains in Volume II, the words, "dictionary binary," on the same line, cause the dictionary for the translation of the data to be transferred to the binary tape so the information will be available when required.

**1.5.3 SETUP PRINT.** The Setup Print control card allows the status of all variables in the model to be printed at the end of the simulation process. Other control cards, "Variable Print" or the "No Variable Print" cards, are used to restrict the number of variables that are printed at the end of the simulation run.

**1.5.4 TRANSLATION MODE.** The Translation Mode control card causes the printout from the simulation process to be printed out, using the engineering nomenclature.

TYPE	DESCRIPTION	VALUE	NØ. ØF EVENTS	DAYS	HOURS	MINUTES	SECONDS
*BINARY ØUTPUT	*****						
*	PRØPRIETARY INFORMATION						
*	SUBJECT TØ						
*	LIMITATION ØF USE CLAUSE						
*	REF. CØNTRACT NAS 8-20016, ART. XIV, XV						
*	*****						
*ID	CHECKØUT MØDEL ENG CUTØFF SYSTEM SIMULATION RUN 2						
*NAMES							
*END NAMES							
*LØGICAL MØDE, Ø2, Ø5.	DICTIONARY BINARY						
*SETUP PRINT							
*TRANSLATION MØDE							

TYPE	DESCRIPTION	VALUE	NØ. ØF EVENTS	DAYS	HOURS	MINUTES	SECONDS
*BEGIN.							
INPUT	BUS1DCØM	1	6				.00
	BUS115A2A41DCØM	1					.00
	BUS115A2A51DCØM	1					.00
INPUT	CØMPUTER RENABLE	1	7				.00
	CØMPGND	1					.00
	CØMPUTERGRØUND	1					.00
ENTER	BUS115A2A41DCØM	1	8				.00
ENTER	BUS115A2A51DCØM	1	7				.00
ENTER	CØMPGND	1	6				.00
ENTER	CØMPUTERGRØUND	1	5				.00
INPUT	BATT115A2ØAØ2	1	4				.00
	BUS1DCØ	1					.01
ENTER	BUS1DCØ	1	4				.01
INPUT	BATT115A1ØAØ1	1	3				.03
	BUS1DCØ	1					.03
ENTER	BUS1DCØ	1	3				.03
INPUT	DCPWRØNCØM	1	2				.03
	PWRSUPPLY353A1	1					.15
	PWRSUPPLY354A1	1					.15
	PWRSUPPLY363A1	1					.05
ENTER	PWRSUPPLY353A1	1	4				.05
	BUS1DCØ	1					.05
	BUSNEGØDØ	1					.05
ENTER	PWRSUPPLY354A1	1	5				.05
	BUS1DCØ	1					.05
	BUSNEGØDØ	1					.05
ENTER	PWRSUPPLY363A1	1	6				.05
	BUS21DCØ	1					.05
	BUSNEGØDØ	1					.05
ENTER	BUS1DCØ	1	7				.05
	BUS1DCØ	1					.05
	BUS1DCØ	1					.05
ENTER	BUSNEGØDØ	1	8				.05
ENTER	BUS1DCØ	1	7				.05
ENTER	BUS1DCØ	1	7				.05
ENTER	BUSNEGØDØ	1	7				.05

EXAMPLE OF DISCRETE NETWORK SIMULATION PROGRAM PRINTOUT  
FIGURE 3-4

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If the "Translation Mode" were not used, the results of the simulation would be printed out in terms of the computer assigned three-letter code names.

**1.5.5 MODEL SIMULATION.** In order to understand the printout from the simulation, it is necessary to have a basic understanding of this program in terms of the model. This explanation is not directly related to the internal operation of the program, itself. The program first establishes an initial condition for the state of the variables in the model. On the basis of this state, it examines all equations in the model and the logic predicts what variables will change state. Since this simulation is to represent real time, after the prediction has been made the program looks up the activation times for the variables changing state, imposes that time delay on the program, and then allows the predicted changes to take place. This process is directly related to the printout, Figure 3-4. "Input" is the indication that the status of this variable is being set by an external command generated by the use of a data card. The code word, "Enter," on Figure 3-4, is the symbol to indicate a change of state that is being generated by the logic of the equations combined with the computer program. On this figure there are several variables listed on the left side which have no code word. The absence of the code word indicates that these are not activities but are predictions of activities as a result of activity described immediately above.

This simulation represents real time. The time of the simulation is printed in the columns on the right hand side of the sheet. The heading on the columns indicate that the time can be described in days, hours, minutes, or seconds. The seconds can be resolved down to the nearest millisecond. The time printed for each activity line represents the actual time. The time listed for the predicted event is the time that the event should occur based upon the time required for that component to activate.

In the center of the page there is the column headed, "Number of Events." This is a bookkeeping function for the Simulator Program and lists the contents of a register which indicate the number of predicted events that have to be satisfied on the basis of either the inputs or actions that have already taken place. At the end of a simulation activity this column will be reduced to zero.

**1.5.6 STATE LIST.** Figure 3-5 is a representative state list, the final printout from the Simulation Program. If a "List" control card is included as the last card in the input deck, the program will summarize the results of the simulation by printing a list giving the state (0 or 1) of all the variables in the model. If the second control card "List 1" is included, only those variables that have a "1" state are listed. This is the example shown in Figure 3-5.

*LIST	AT	3005	NØ.	3		
BATT115A10NØ1					=	1.
BATT115A20NØ2					=	1.
COMPUTERENABLE					=	1.
DCPWØNCØM					=	1.
LAUNCHPRESSØK					=	1.
LØXFUELLØADED					=	1.
PWRTRANSW115A1S1					=	1.
THRUSTØKENGØ1					=	1.
THRUSTØKENGØ2					=	1.
THRUSTØKENGØ3					=	1.
THRUSTØKENGØ4					=	1.
THRUSTØKENGØ5					=	1.
NØDE115A3E268					=	1.
NØDE115A3J23E					=	1.
NØDE115A3J23N					=	1.
NØDE115A3J24F					=	1.
NØDE115A3J24W					=	1.
NØDE115A3J26C					=	1.
NØDE115A3J2621					=	1.
NØDE115A3J263					=	1.
NØDE115A3J27E					=	1.
NØDE115A3J27N					=	1.
NØDE5A6J16R					=	1.
NØDE5A7J16X					=	1.
NØDE5A7J16Z					=	1.
NØDE5A7J41AA					=	1.
NØDE5A7J41BB					=	1.
NØDE6A3J12SD					=	1.
NØDE6A3J12SH					=	1.
NØDE6A3J29ST					=	1.
NØDE6A4J11X					=	1.
NØDE6A4J11Z					=	1.
NØDE6A4J21CC					=	1.
NØDE6A4J21CD					=	1.
NØDE6A4J27E					=	1.
NØDE7A3K5C1					=	1.
LEG3N115A3E268					=	1.
LEG3N115A3J23E					=	1.
LEG3N115A3J23N					=	1.
LEG5N115A3J24F					=	1.
LEG5N115A3J24W					=	1.
LEG4N115A3J26C					=	1.
LEG2N115A3J263					=	1.
LEG4N115A3J263					=	1.
LEG1N115A3J2621					=	1.
LEG2N115A3J27E					=	1.
LEG3N115A3J27N					=	1.
LEG2N5A7J16R					=	1.
LEG3N5A7J16X					=	1.

EXAMPLE OF DISCRETE NETWORK SIMULATION PRINTOUT OF STATE LIST

FIGURE 3-5

## GENERAL DYNAMICS | CONVAIR

Additional state lists may be created during the simulation process by the use of control cards at the beginning of the run. The control card "list" at (time) will cause a state list as described above to be printed for each time listed.

The use of a control card, "Cycle List," will cause a state list to be printed for every time period or change of state that occurs during the total simulation program.

### 1.6 DNS PREPROCESSOR EDITOR PROGRAM

The Preprocessor Editor Program reads the binary model tape output from the DNS Preprocessor Program, and prints out specified reference tables according to the control cards used. The reference tables describe the variable interdependencies in a DNS model. A choice of three program printouts is available.

1.6.1 The Index control card produces an alphabetical list of all coded variables, the corresponding internal code numbers, and whether a variable is an initiator (is defined only in the right hand side of the equation), or a terminal (is defined on both sides of the equal sign in the equation). This list is followed by a "Variable Reference" table in which each variable name is printed out, followed by a list of functions in which it occurs.

1.6.2 The Index Full control card creates two additional tables which printout between the two above. They are the "Variable-Terminal" table and the "Terminal-Variable" table. The Terminal-Variable table lists the terminals on the left hand side of the page and then follows each terminal with a list of variables that are directly or indirectly affected by the subject terminal. The Variable-Terminal list prints the variable on the left hand side of the page followed by a listing of the terminals on which that variable will have effect.

1.6.3 The Index Logic control card prints only the Variable-Terminal and Terminal-Variable tables. Figure 3-6 is a sample of the "Variable Reference Table." Appendix C is the complete "Index Logic Preprocessor Editor output for the complete model.



# VARIABLE REFERENCE TABLE

VARIABLE	FUNCTIONS
00245 AGI	C0N .
00246 AGJ	0KL .
00247 AGK	C0N .
00250 AGL	BKM .
00251 AGM	BMC .
00252 AGN	BDF ,BDJ ,BGS .
00253 AG0	AZE ,BGP ,BLF .
00254 AGP	BGL ,BLI .
00255 AGQ	BGM ,BLE .
00256 AGR	AWE ,AW0 ,CJB .
00257 AGS	AVY ,AXW ,BLM ,0LN ,0L0 ,BLP ,BLQ ,BLR .
00260 AGT	BLX ,BLY .
00261 AGU	BKZ ,BLJ .
00262 AGV	AVZ ,AZJ ,C0W ,C0X .
00263 AGW	BMK ,CIT .
00264 AGX	AXH ,AYL ,BER .
00265 AGY	AXG ,0BJ ,BEX .
00266 AGZ	AXK ,BBT ,BE0 .
00267 AHA	AXM ,BB0 ,BEL .
00270 AHB	AXP ,0BD ,BEU .
00271 AHC	AWQ ,AWT ,AWW ,AXB ,AXD ,AZP ,AZR ,AZU ,AZX ,BAA .
00272 AHD	BEC ,CMY .
00273 AHE	B0W ,CMX .
00274 AHF	AWF ,BMM ,BMN .
00275 AHG	B0X ,00I ,00J .
00276 AHH	B0Z ,00G .
00277 AHI	B0B ,00H .
00300 AHJ	BEG ,00B .
00301 AHK	BEH ,00K ,00L .

EXAMPLE OF PREPROCESSOR EDITOR PRINTOUT

## 2/SIMULATION OF ENGINE CUTOFF SYSTEM

## 2.1 ENGINES RUNNING

In the previous section we have described the programs that are used to accomplish a system simulation. We have described the methodology used to write the logic equations in Volume I and have shown in Appendix B the complete logical model of the Engine Cutoff System. The logic equations that describe the system are written to indicate the de-energized state. The DNS model represents a static system and additional inputs are required to cause the DNS model to become a dynamic system. In order to simulate the Engine Cutoff System, we must first cause the model to represent the networks in the "All Engine Running Condition." Based upon an analysis of the networks and the interface where the model was terminated, a list of inputs was defined (Table 3-IV) that activate the logic model and cause this model to represent the Engines Running Condition.

The inputs and activation times listed in Table 3-IV are put into the model, the simulation is activated and the networks go to the Engines Running Condition. The model starts with all variables in a "zero" or "off" condition. As a result of the initial input of 30 variables, the model then goes to a state where there are 305 variables in the "on" or "1" state, as summarized in Table 3-V.

# GENERAL DYNAMICS | CONVAIR

TABLE 3-IV  
INPUTS INTO STATIC MODEL  
TO PRODUCE ALL ENGINES RUNNING CONDITION

ABB	= 1 AT 0.	LAUNCH PRES OK
ABC	= 1 AT 0.	LOXFUELLOADED
AAE	= 1 AT 0.	COMPUTER ENABLE
BSU	= 1 AT 0.	BUS1DCOM
BTE	= 1 AT 0.	BUS1D119
ABM	= 1 AT 0.	PWRTRANSW115A1S1
CXC	= 1 AT 0.	LOXENG CUTOFFSW115A46NO1
CXD	= 1 AT 0.	LOXENG CUTOFFSW115A47NO2
CXE	= 1 AT 0.	LOXENG CUTOFFSW115A48NO3
CXF	= 1 AT 0.	LOXENG CUTOFFSW115A49NO4
CXG	= 1 AT 0.	LOXENG CUTOFFSW115A50NO5
BYX	= 1 AT 0.	COIL5A7K470J14PPSJ
BYY	= 1 AT 0.	COIL5A7K471J14PPSS
BYZ	= 1 AT 0.	COIL5A7K472J14PPSZ
BZF	= 1 AT 0.	COIL5A7K511J19AB
BZH	= 1 AT 0.	COIL5A7K515J19PPSJ
BZI	= 1 AT 0.	COIL5A7K516J19PPSS
BZJ	= 1 AT 0.	COIL5A7K517J19PPSZ
BZK	= 1 AT 0.	COIL5A7K518J19PPGG
BZN	= 1 AT 0.	COIL5A7K524J4PPSS
BZO	= 1 AT 0.	COIL5A7K525J4PPSZ
BZP	= 1 AT 0.	COIL5A7K526J4PPGG
AAD	= 1 AT 10.	BATT115A20NO2
AAC	= 1 AT 30.	BATT115A10NO1
AAG	= 1 AT 50.	DC PWR ON COMMAND
ABA	= 1 AT 20.	IGNITION SIGNAL
BYX	= 0 AT 3000.	COIL5A7K470J14PPSJ
BYY	= 0 AT 3000.	COIL5A7K471J14PPSS
BYZ	= 0 AT 3000.	COIL5A7K472J14PPSZ
ABA	= 0 AT 3000.	IGNITION SIGNAL

# GENERAL DYNAMICS | CONVAIR

TABLE 3-V

## SUMMARY OF ALL ENGINE RUNNING CONDITION, 1 STATE LIST

Nodes	42
Legs	45
Buses	24
Coils	24
Contacts	42
Discrete In	17
Valves	35
Lights	19
Switches	25
Misc.	<u>32</u>
Total	305

A list of the actual components that are activated in the Engines Running Condition is shown in Table 3-VI. Appendix D is the computer printout of the simulation that establishes all engines running.

ALL ENGS RUNNING LITE GREEN
BUSNEG1D2
BUS115A2A41DC0M
BUS115A2A51DC0M
BUS1DC0M
BUS1D10
BUS1D11
BUS1D112
BUS21D118
BUS1D12
BUS1D20
BUS1D21
BUS1D110
BUS1D11
BUS1D119
BUSNEG1D1
BUS1D210
BUS1D211
BUS21D110
BUS21D113
BUS21D115
BUS21D119
BUS21D120
BUS21D121
BUSNEG21D1
C0IL115A9K11
C0IL115A9K21
C0IL115A9K31
C0IL5A1K164J22PPSZ
C0IL5A2K163J29TU
C0IL5A2K164J36TU
C0IL5A4K371J20PPSZ
C0IL5A6K404J17PPSZ
C0IL5A6K405J17TU
C0IL5A7K440J31PPSJ
C0IL5A7K440J32PPGG
C0IL5A7K440J32PPSJ
C0IL5A7K440J32PPSS
C0IL5A7K440J32PPSZ
C0IL5A7K511J19A8
C0IL5A7K515J19PPSJ

C0IL5A7K516J19PPSS
C0IL5A7K517J19PPSZ
C0IL5A7K518J19PPGG
C0IL5A7K522J4S8SC
C0IL5A7K523J4PPSJ
C0IL5A7K524J4PPSS
C0IL5A7K525J4PPSZ
C0IL5A7K526J4PPGG
COMPGND
COMPUTERGRWUND
327D186
327D197
327D1265
327D1267
327D1307
327D1308
327D1336
327D1338
327D1423
327D1425
327D1427
327D11200
327D11212
327D11222
327D11333
327D11334
327D11335
FLTC08BM0N115A51UNITA
FLTC08BM0N115A51UNITB
FLTC08BM0N115A51UNITC
FLTC08BM0N115A52UNITA
FLTC08BM0N115A52UNITB
FLTC08BM0N115A52UNITC
FLTC08BM0N115A53UNITA
FLTC08BM0N115A53UNITB
FLTC08BM0N115A53UNITC
FLTC08BM0N115A54UNITA
FLTC08BM0N115A54UNITB
FLTC08BM0N115A54UNITC
FLTC08BM0N115A55UNITA
FLTC08BM0N115A55UNITB

FLTC08BM0N115A55UNITC
FUELPREVLVN01ENG1
FUELPREVLVN02ENG1
FUELPREVLVN01ENG2
FUELPREVLVN02ENG2
FUELPREVLVN01ENG3
FUELPREVLVN02ENG3
FUELPREVLVN01ENG4
FUELPREVLVN02ENG4
FUELPREVLVN01ENG5
FUELPREVLVN02ENG5
FUELPREVLVN01ENG6
FUELPREVLVN02ENG6
LITE308A1DS14G
LITE308A1DS35G
LITE308A1DS36G
LITE308A1DS87G
LITE388A5DS7W
LITE388A5DS14W
LITE388A6DS10W
LITE400A12DS63W
LITE400A12DS79W
LITE400A12DS81W
LITE400A12DS83W
LITE400A12DS114G
LITE400A12DS116G
LITE400A12DS118G
LITE400A12DS120G
LITE400A12DS136G
LITE400A12DS137G
LITE400A12DS138G
LITE400A12DS139G
L0XENGCU0FFSW115A46N01
L0XENGCU0FFSW115A47N02
L0XENGCU0FFSW115A48N03
L0XENGCU0FFSW115A49N04
L0XENGCU0FFSW115A50N05
L0XPREVLVENG1
L0XPREVLVENG2
L0XPREVLVENG3
L0XPREVLVENG4
L0XPREVLVENG5
MAINFUELVLV1ENG1

MAINFUELVLV2ENG1
MAINFUELVLV1ENG2
MAINFUELVLV2ENG2
MAINFUELVLV1ENG3
MAINFUELVLV2ENG3
MAINFUELVLV1ENG4
MAINFUELVLV2ENG4
MAINFUELVLV1ENG5
MAINFUELVLV2ENG5
MAINL0XVLVN01ENG1
MAINL0XVLVN02ENG1
MAINL0XVLVN01ENG2
MAINL0XVLVN02ENG2
MAINL0XVLVN01ENG3
MAINL0XVLVN02ENG3
MAINL0XVLVN01ENG4
MAINL0XVLVN02ENG4
MAINL0XVLVN01ENG5
MAINL0XVLVN02ENG5
P0SSWMAINFUELVLV1ENG1
P0SSWMAINFUELVLV2ENG1
P0SSWMAINL0XVLVN01ENG1
P0SSWMAINL0XVLVN02ENG1
PWRSUPPLY353A1
PWRSUPPLY354A1
PWRSUPPLY360A1
THRUST0KPRESSW101N01
THRUST0KPRESSW101N02
THRUST0KPRESSW101N03
THRUST0KPRESSW102N01
THRUST0KPRESSW102N02
THRUST0KPRESSW102N03
THRUST0KPRESSW103N01
THRUST0KPRESSW103N02
THRUST0KPRESSW103N03
THRUST0KPRESSW104N01
THRUST0KPRESSW104N02
THRUST0KPRESSW104N03
THRUST0KPRESSW105N01
THRUST0KPRESSW105N02
THRUST0KPRESSW105N03

TABLE 3-VI STATE LIST "1" WITH MODEL IN THE ALL ENGINES RUNNING CONFIGURATION

## GENERAL DYNAMICS | CONVAIR

### 2.2 ENGINE CUTOFF

After establishing the engines running, the activities listed in Table 3-VII were put in the simulation process representing a possible Engine Cutoff Mode. In this case it was the signal for "Thrust OK Pressure Switch."

TABLE 3-VII  
INPUTS TO ALL ENGINE RUNNING STATE FOR  
THRUST NOT OK ENGINE CUTOFF

*BEGIN.		ENG. NO 1 THRUST NOT OK
CZX	= 0 at 5000.	THRUST OK PRESSW101N02
ACR	= 1 at 5000.	COUNTDOWN SEQUENCE TIME PLUS 5 SECS.
CZY	= 0 at 6000.	THRUST OK PRESSW101N03
ABY	= 1 at 20000.	SWITCH SELECTOR CHANNEL 3 OUTPUT
ABO	= 1 at 50000.	COUNTDOWN SEQUENCE RESET

At the end of this sequence a new state list was printed, as shown in Table 3-IX. This is summarized in Table 3-VIII. Starting with the model "Off," or in the "0" state, 30 inputs turned on 305 variables. Five additional inputs simulated engine cutoff and turned on an additional 580 variables, while turning off the majority of the variables on when the engines are running. Appendix E is the computer printout of the Engine Cutoff Simulation.

There are several conditions which will cause engine cutoff. The following additional runs were made, with the inputs as listed in each case, and the system in the All Engines Running Condition prior to the start of each case.

1. Engine Cutoff by Fuel Bilevel Cutoff Sensor:  
Inputs -- Switch Selector Channel 9 Output  
Fuel Bilevel Sensor 115A76
2. Engine Cutoff from Thrust Not OK Pressure Switch:  
Inputs -- Thrust OK Pressure Switch 102N01  
Thrust OK Pressure Switch 102N2  
Switch Selector Channel 3 Output
3. Engine Cutoff from Lox Pressure Switches:  
Inputs -- Lox Engine Cutoff Switch 115A48 No. 2  
Lox Engine Cutoff Switch 115A49 No. 4

## GENERAL DYNAMICS | CONVAIR

Lox Engine Cutoff Switch 115A50 No. 5  
Switch Selector Channel 8 Output  
Switch Selector Channel 9 Output

4. Engine Cutoff from Lox Level Sensors  
Inputs -- Lox Level Sensor No. 1 113A1  
Lox Level Sensor No. 2 118A2  
Switch Selector Channel 9 Output
5. Engine 3 Cutoff from Rough Combustion Y and Z Axis  
Inputs -- Engine 3 Rough Combustion Y Axis  
Engine 3 Rough Combustion Z Axis

TABLE 3-VIII  
A SUMMARY OF ALL ENGINE CUTOFF

### CONDITION, "1" STATE LIST

Nodes	112
Legs	133
Buses	24
Coils	68
Contacts	110
Discretes In	24
Lights	32
Switches	8
Solenoids	15
Timers	12
Misc.	42
<hr/>	
Total	580

BUSNEG102	C01L5A2K163J29TU	327D1422	LITE400A12DS197R
BUS115A2A1DC0M	C01L5A2K164J36TU	327D1424	LITE400A12DS201R
BUS115A2A51DC0M	C01L5A4K359J17JK	327D1426	LITE400A12DS216R
BUS1DC0M	C01L5A4K359J27TU	327D11200	LITE400A12DS247R
BUS1D10	C01L5A4K359J31JK	327D11212	LITE400A12DS263R
BUS1D11	C01L5A4K359J31S8SC	327D11217	LØXENGCU0FFSW115A46NØ1
BUS1D112	C01L5A4K359J31TU	327D11218	LØXENGCU0FFSW115A47NØ2
BUS21D118	C01L5A4K371J20PPSZ	327D11219	LØXENGCU0FFSW115A48NØ3
BUS1D12	C01L5A4K371J20PPSZ	327D11220	LØXENGCU0FFSW115A49NØ4
BUS1D20	C01L5A6K400J18AB	327D11221	LØXENGCU0FFSW115A50NØ5
BUS1D21	C01L5A6K401J17AB	327D11222	PØSSW115A31ENG1FPV
BUS1D110	C01L5A6K402J17S8SC	ENGCU0FFCØMPLÈTE	PØSSW115A32ENG1FPV
BUS1D111	C01L5A6K403J17PPSJ	FLTCØMBMØN115A51UNITA	PØSSW115A41ENG1LPV
BUS1D119	C01L5A6K404J17PPSZ	FLTCØMBMØN115A51UNITB	PØRSUPPLY353A1
BUSNEG101	C01L5A7K172J32JK	FLTCØMBMØN115A51UNITC	PØRSUPPLY354A1
BUS1D210	C01L5A7K359J14S8SC	FLTCØMBMØN115A52UNITA	PØRSUPPLY360A1
BUS1D211	C01L5A7K359J51TU	FLTCØMBMØN115A52UNITB	SØLENG1CØNTVLVSTØP
BUS21D110	C01L5A7K440J31PPSJ	FLTCØMBMØN115A52UNITC	SØLENG2CØNTVLVSTØP
BUS21D113	C01L5A7K440J32PPGG	FLTCØMBMØN115A53UNITA	SØLENG3CØNTVLVSTØP
BUS21D115	C01L5A7K440J32PPSJ	FLTCØMBMØN115A53UNITB	SØLENG4CØNTVLVSTØP
BUS21D119	C01L5A7K440J32PPSS	FLTCØMBMØN115A53UNITC	SØLENG5CØNTVLVSTØP
BUS21D120	C01L5A7K440J32PPSZ	FLTCØMBMØN115A54UNITA	SØLENGØ1D115A21
BUS21D121	C01L5A7K450J30S8SC	FLTCØMBMØN115A54UNITB	SØLENGØ1D115A22
BUSNEG2101	C01L5A7K464J7PPSJ	FLTCØMBMØN115A54UNITC	SØLENGØ1D115A23
CØ1L115A3A2K14	C01L5A7K478J21PPSZ	FLTCØMBMØN115A55UNITA	SØLENGØ1D115A24
CØ1L115A3A2K24	C01L5A7K511J19AB	FLTCØMBMØN115A55UNITB	SØLENGØ1D115A25
CØ1L115A3A9K12	C01L5A7K515J19PPSJ	FLTCØMBMØN115A55UNITC	SØLENGØ1D115A92
CØ1L115A3A9K13	C01L5A7K516J19PPSS	LITE308A1DS14G	SØLENGØ1D115A93
CØ1L115A3A9K15	C01L5A7K517J19PPSZ	LITE308A1DS35G	SØLENGØ1D115A94
CØ1L115A3A9K22	C01L5A7K518J19PPGG	LITE308A1DS36G	SØLENGØ1D115A95
CØ1L115A3A9K23	C01L5A7K524J4PPSS	LITE308A1DS88R	SØLENGØ1D115A96
CØ1L115A3A9K25	C01L5A7K525J4PPSZ	LITE308A1DS97R	STØPFIRINGCØMMAND
CØ1L115A3K1	C01L5A7K526J4PPGG	LITE388A5DS56G	STØPIGNIT1ØNSEQ
CØ1L115A3K2	C01L5A7K531J11PPSJ	LITE388A5DS7W	TIMER115A4A1NØ1
CØ1L115A3K3	C01L5A7K532J11PPSS	LITE388A5DS9G	TIMER115A4A1NØ2
CØ1L115A3K37	C01L5A7K546J12PPSJ	LITE388A5DS11G	TIMER115A4A2NØ1
CØ1L115A3K4	C01L5A7K546J17TU	LITE388A5DS13G	TIMER115A4A2NØ2
CØ1L115A3K5	C01L5A7K547J12PPSZ	LITE388A5DS14W	TIMER115A4A3NØ1
CØ1L115A4K61	C01L5A7K547J12PPSS	LITE388A5DS15G	TIMER115A4A5NØ2
CØ1L115A4K62	CØMPGND	LITE388A6DS10W	TIMER115A4A6NØ1
CØ1L115A4K63	CØMPUTERGRØUND	LITE400A12DS63W	TIMER115A4A6NØ2
CØ1L115A4K64	327D166	LITE400A12DS80G	TIMER115A4A7NØ1
CØ1L115A4K65	327D173	LITE400A12DS82G	TIMER115A4A7NØ2
CØ1L115A4K71	327D186	LITE400A12DS84G	TIMER5A15K135
CØ1L115A4K72	327D187	LITE400A12DS115W	TIMER5A15A7K441
CØ1L115A4K73	327D188	LITE400A12DS117W	TIMER115A4A1NØ1ØUT
CØ1L115A4K74	327D190	LITE400A12DS119W	TIMER115A4A1NØ2ØUT
CØ1L115A4K75	327D197	LITE400A12DS121W	TIMER115A4A2NØ1ØUT
LCØ1L384A4K15L20	327D1264	LITE400A12DS123R	TIMER115A4A2NØ2ØUT
LCØ1L384A4K15L21	327D1266	LITE400A12DS139G	TIMER115A4A3NØ1ØUT
LCØ1L384A4K16L21	327D1307	LITE400A12DS140R	TIMER115A4A5NØ2ØUT
LCØ1L384A4K17L21	327D1308	LITE400A12DS154R	TIMER115A4A6NØ1ØUT
CØ1L5A1K164J22PPSZ	327D1337	LITE400A12DS170R	TIMER115A4A6NØ2ØUT
	327D1339	LITE400A12DS185R	

STATE LIST "1" AFTER ENGINE CUTOFF FROM THRUST OK PRESSURE SWITCHES

TABLE 3-IX



## 2.3 INCORPORATING ENGINEERING CHANGES

2.3.1 Discrete Network Simulation of a hardware system is an analytical tool which has many applications. The logic model represents the actual hardware system. In a research and development program, the hardware is subject to a series of engineering changes based upon analysis and testing of the original design. If simulation is to be used effectively it must represent the latest hardware configuration. The value of DNS as an analytical tool is related to the ability to incorporate changes into the DNS model rapidly, accurately, and economically. The methods used to build the DNS model were designed to allow for subsequent incorporation of changes into the model. To incorporate a change in the DNS model, the following steps are required:

1. Analyze the old and new schematics to define where the change affects the existing model and how this interface can be defined.
2. Write the logic equations for the new networks required by the change.
3. Prepare time-cards for all new variables introduced by the change.
4. Insert the new equations and time-cards into the card deck that represents the logic model and remove the cards for all variables no longer present in the network.
5. Prepare a new DT&C tape from the card deck. The new DT&C tape is then run with the DNS Preprocessor Program and the output tape from this program represents the new model ready for use with the Simulation Program.

2.3.2 To demonstrate this capability, a change was defined by the Quality and Reliability Assurance Laboratory for incorporation into the existing model of the S1C Engine Cutoff System.

1. Sheet 37 of Drawing 60B55701, Revision A, gave a new circuit for the Engine No. 1, Thrust OK Pressure Switches. In the ESE, Schematics 616, 617, 618, 619, 619A, 619B and 620 were affected.
2. At 1:00 p.m. on a Wednesday, the analysis and preparation of the new equations commenced. This effort continued until noon, Friday. This includes writing equations, keypunching, (equations and time-cards) and checking. All keypunching was accomplished by the analyst.
3. Table 3-X summarized the results.

## GENERAL DYNAMICS | CONVAIR

TABLE 3-X  
NEW EQUATIONS WRITTEN

Nodes	20
Legs	51
Relay Coils	7
Relay Contacts	13
Lights	4
DI's	<u>3</u>
Total	98
Total Cards	
Keypunched	347

4. Beginning at noon, Friday, the new cards were listed for reference and then inserted into the card deck representing the Engine Cutoff System. The cards for the equations describing the old circuit were removed.
5. The new deck (set of equations) was run with the DNS Down Translation and Culling (DT&C) program Friday afternoon. The output tape from the DT&C program was run with the DNS Preprocessor Program Friday evening. The output tape from the Preprocessor contains the new DNS model with the changes incorporated.
6. This total effort required two and one-quarter (2.25) men from noon, Wednesday, until Friday evening, or 20 working hours. The task could have been accomplished in one and one-half (1.5) days if trained keypunch support had been used.

## GENERAL DYNAMICS | CONVAIR

### 3/COMPONENT MALFUNCTION SIMULATION

The insertion of component failures into the simulation was one of the first applications for DNS. The comparison of the normal with the failure provides the data for fault isolation. To demonstrate the insertion of malfunctions into the DNS model, the following runs were made.

With the complete model of the Engine Cutoff System, the inputs listed were used to establish the model in the "Power On" condition.

AAE = 1 at 20	Computer Enable
BSU = 1 at 30	Bus 1DCOM
BTE = 1 at 40	Bus 1D 119
AAC = 1 at 90	BATT 115A10 No. 1
AAD = 1 at 100	BATT 115A20 No. 2
AAG = 1 at 120	DC Power On Command

The complete state list for Power On is shown in Appendix F.

The normal operation of the system when Discrete Out 436, Start Engine No. 1 Control Valve, is energized, was selected as the configuration of the system against which component failure results would be compared. When Discrete Out (DO 436) was input into the simulation run, a new state "1" list was made, as shown in Appendix F and as summarized in Table 3-XI.

For the simulation from which the following state lists were made, the variable print option was used. This option allows only those variables that are desired to be shown in the printout. In these lists only Lights, DI's, DO's, and a few other selected variables were allowed to print. These include all the monitoring points that are available in this part of the system. Table 3-XII is a condensed "1" state list for the Power On configuration and it can be noted that there are 11 DI's and 14 Lights on this list.

# GENERAL DYNAMICS | CONVAIR

TABLE 3-XI  
SUMMARY OF POWER ON, "1" STATE LIST

<u>Variable</u>	<u>Power On Configuration</u>	<u>DO 436 Energized</u>
Nodes	57	58
Legs	74	75
Buses	23	23
Coils	29	26
Contacts	39	42
Discrete In	13	14
Valves	0	4
Lights	14	15
Switches	0	4
Misc.	24	25
	—	—
TOTAL	273	286

## 3.1 DIODE SHORTED

With the model in the Power On configuration, a diode, 115A3A4CR44S, was shorted to see the effect this would have on Engine Cutoff Network in a static checkout condition. The condensed state list for this condition is shown in Table 3-XIII. The number of Lights On increased from 14 to 38 and the number of DI's increased from 11 to 26. From this it can be seen that this diode is a critical item in the network.

## 3.2 RELAY CONTACT FAILURE

The condensed state list for the simulation of DO 436 is the basis of comparison for failure effects. The run was repeated, setting the contacts of a related coil, CONT5A7K440J32SQSR, to zero, a simulated failure. Table 3-XIV gives the condensed state list for the two runs. It can be seen that there is a definite difference in the two lists due to the failure of the contact.

# GENERAL DYNAMICS | CONVAIR

TABLE 3-XII  
CONDENSED STATE LIST FOR POWER ON

<u>C0IL5A7K440J32PPSJ</u>
<u>C0NT5A7K440J32SMSN</u>
<u>C0NT5A7K440J32SQSR</u>
<u>327DI97</u>
<u>327DI264</u>
<u>327DI266</u>
<u>327DI307</u>
<u>327DI308</u>
<u>327DI337</u>
<u>327DI339</u>
<u>327DI423</u>
<u>327DI425</u>
<u>327DI427</u>
<u>327DI1200</u>
<u>327DI1212</u>
<u>327DI1222</u>
<u>LITE308A1DS14G</u>
<u>LITE308A1DS35G</u>
<u>LITE308A1DS36G</u>
<u>LITE388A5DS7W</u>
<u>LITE388A5DS14W</u>
<u>LITE388A6DS10W</u>
<u>LITE400A12DS63W</u>
<u>LITE400A12DS79W</u>
<u>LITE400A12DS81W</u>
<u>LITE400A12DS83W</u>
<u>LITE400A12DS115W</u>
<u>LITE400A12DS117W</u>
<u>LITE400A12DS119W</u>
<u>LITE400A12DS121W</u>

# GENERAL DYNAMICS | CONVAIR

TABLE 3-XIII  
CONDENSED "1" STATE LIST WITH POWER ON  
AND DIODE 115A3A4CR44 SHORTED

<u>CØIL5A7K440J32PPSJ</u>	<u>LITE308A1DS89R</u>
<u>CØNT5A7K440J32SMSN</u>	<u>LITE308A1DS90R</u>
<u>CØNT5A7K440J32SQSR</u>	<u>LITE308A1DS91R</u>
<u>DIØDE115A3A4CR44S</u>	<u>LITE308A1DS92R</u>
<u>327DI64</u>	<u>LITE308A1DS97R</u>
<u>327DI73</u>	<u>LITE388A5DS6G</u>
<u>327DI75</u>	<u>LITE388A5DS7W</u>
<u>327DI77</u>	<u>LITE388A5DS9G</u>
<u>327DI79</u>	<u>LITE388A5DS11G</u>
<u>327DI81</u>	<u>LITE388A5DS13G</u>
<u>327DI87</u>	<u>LITE388A5DS14W</u>
<u>327DI88</u>	<u>LITE388A5DS15G</u>
<u>327DI90</u>	<u>LITE388A6DS10W</u>
<u>327DI97</u>	<u>LITE400A12DS63W</u>
<u>327DI264</u>	<u>LITE400A12DS79W</u>
<u>327DI266</u>	<u>LITE400A12DS81W</u>
<u>327DI307</u>	<u>LITE400A12DS83W</u>
<u>327DI308</u>	<u>LITE400A12DS115W</u>
<u>327DI337</u>	<u>LITE400A12DS117W</u>
<u>327DI339</u>	<u>LITE400A12DS119W</u>
<u>327DI423</u>	<u>LITE400A12DS121W</u>
<u>327DI425</u>	<u>LITE400A12DS123R</u>
<u>327DI427</u>	<u>LITE400A12DS135R</u>
<u>327DI1200</u>	<u>LITE400A12DS140R</u>
<u>327DI1212</u>	<u>LITE400A12DS154R</u>
<u>327DI1217</u>	<u>LITE400A12DS170R</u>
<u>327DI1218</u>	<u>LITE400A12DS171R</u>
<u>327DI1219</u>	<u>LITE400A12DS185R</u>
<u>327DI1220</u>	<u>LITE400A12DS201R</u>
<u>327DI1221</u>	<u>LITE400A12DS202R</u>
<u>327DI1222</u>	<u>LITE400A12DS216R</u>
<u>LITE308A1DS14G</u>	<u>LITE400A12DS247R</u>
<u>LITE308A1DS35G</u>	<u>LITE400A12DS263R</u>
<u>LITE308A1DS36G</u>	<u>LITE400A12DS264R</u>
<u>LITE308A1DS88R</u>	<u>SØLENG1CØNTVLVSTØP</u>

# GENERAL DYNAMICS | CONVAIR

TABLE 3-XIV  
CONDENSED "1" STATE LISTS WITH DO 436 ENERGIZED  
AND CONT5A7K440J32SQSR FAILED

## NORMAL

C0IL5A7K440J32PPSJ  
 C0IL5A7K447J31PPGG  
 C0NT5A7K440J32SMSN  
 C0NT5A7K440J32SQSR  
 C0NT5A7K447J31JJJK  
 327DI97  
 327DI265  
 327DI267  
 327DI307  
 327DI308  
 327DI336  
 327DI338  
 327DI423  
 327DI425  
 327DI427  
 327DI444  
 327DI1200  
 327DI1212  
 327DI1222  
 327D0436  
 LITE308A1DS14G  
 LITE308A1DS35G  
 LITE308A1DS36G  
 LITE388A5DS7W  
 LITE388A5DS14W  
 LITE388A6DS10W  
 LITE400A12DS63W  
 LITE400A12DS79W  
 LITE400A12DS81W  
 LITE400A12DS83W  
 LITE400A12DS114G  
 LITE400A12DS116G  
 LITE400A12DS118G  
 LITE400A12DS120G  
 LITE400A12DS122G  
 MAINFUELVLV1ENG1  
 MAINFUELVLV2ENG1  
 MAINL0XVLVN01ENG1  
 MAINL0XVLVN02ENG1  
 P0SSWMAINFUELVLV1ENG1  
 S0LENG1C0NTVLVSTART

## CONT5A7K440J32SQSR FAILED

C0IL5A7K440J32PPSJ  
 C0NT5A7K440J32SMSN  
 327DI97  
 327DI264  
 327DI266  
 327DI307  
 327DI308  
 327DI337  
 327DI339  
 327DI423  
 327DI425  
 327DI427  
 327DI1200  
 327DI1212  
 327DI1222  
 327D0436  
 LITE308A1DS14G  
 LITE308A1DS35G  
 LITE308A1DS36G  
 LITE388A5DS7W  
 LITE388A5DS14W  
 LITE388A6DS10W  
 LITE400A12DS63W  
 LITE400A12DS79W  
 LITE400A12DS81W  
 LITE400A12DS83W  
 LITE400A12DS115W  
 LITE400A12DS117W  
 LITE400A12DS119W  
 LITE400A12DS121W

## GENERAL DYNAMICS | CONVAIR

### 3.3 RELAY COIL FAILURE

Table 3-XV compares the normal DO 436 state to the results of failing a coil, namely, COIL5A7K447J31PPGG. As in the previous run, there is a definite change due to the coil failure. However, a detailed comparison with Table 3-XIV shows that the malfunction results are the same and additional variables would have to be compared to differentiate between the two failures.

### 3.4 CONNECTOR PIN FAILURE

Table 3-XVI compares the normal DO 436 state to the results of failing a pin in a connector, PIN6A4J10S. This is the same as failing a complete leg of a circuit. Analysis will show that DI 444, Engine No. 1 Solenoid Start, and Light 400A12DS122G, are off. This is a limited but definite failure indication.

### 3.5 ENGINE NO. 1 START SOLENOID FAILURE

The effect of preventing the Start Solenoid, SOLENG1CONTVLVSTART, from operating when DO 436 was input is shown in Table 3-XVII. While the number of activities is approximately the same, the indicators activated are different. There are eight DI's and six Lights that are different between the two runs. Notice, also, that the Main Lox and Fuel Valves did not activate.

### 3.6 MAIN FUEL VALVE POSITION SWITCH FAILURE

Simulation of checkout using DO 436 was repeated, while preventing Main Fuel Valve No. 1 Position Switch from activating, (a failure). Comparison of the condensed state lists, Table 3-XVIII, indicates that for the normal run, DI 336 and Light DS118E are on, while the position switch failure caused these two indicators to stay off, and DI 337 and Light DS119W to come on. These indicators are directly connected to the position switch and illustrate that the DNS model does represent the hardware.



# GENERAL DYNAMICS | CONVAIR

TABLE 3-XV  
CONDENSED "1" STATE LISTS WITH DO 436 ENERGIZED  
AND COIL5A7K447J31PPGG FAILED

NORMAL	COIL5A7K447J31PPGG FAILED
C0IL5A7K440J32PPSJ	C0IL5A7K440J32PPSJ
C0IL5A7K447J31PPGG	C0NT5A7K440J32SMN
C0NT5A7K440J32SMN	C0NT5A7K440J32SQR
C0NT5A7K440J32SQR	327DI97
C0NT5A7K447J31JJK	327DI264
327DI97	327DI266
327DI265	327DI307
327DI267	327DI308
327DI307	327DI337
327DI308	327DI339
327DI336	327DI423
327DI338	327DI425
327DI423	327DI427
327DI425	327DI1200
327DI427	327DI1212
327DI444	327DI1222
327DI1200	327D0436
327DI1212	LITE308A1DS14G
327DI1222	LITE308A1DS35G
327D0436	LITE308A1DS36G
LITE308A1DS14G	LITE388A5DS7W
LITE308A1DS35G	LITE388A5DS14W
LITE308A1DS36G	LITE388A6DS10W
LITE388A5DS7W	LITE400A12DS63W
LITE388A5DS14W	LITE400A12DS79W
LITE388A6DS10W	LITE400A12DS81W
LITE400A12DS63W	LITE400A12DS83W
LITE400A12DS79W	LITE400A12DS115W
LITE400A12DS81W	LITE400A12DS117W
LITE400A12DS83W	LITE400A12DS119W
LITE400A12DS114G	LITE400A12DS121W
LITE400A12DS116G	
LITE400A12DS118G	
LITE400A12DS120G	
LITE400A12DS122G	
MAINFUELVLV1ENG1	
MAINFUELVLV2ENG1	
MAINL0XVLVN01ENG1	
MAINL0XVLVN02ENG1	
P0SSWMAINFUELVLV1ENG1	
S0LENG1C0NTVLVSTART	

# GENERAL DYNAMICS | CONVAIR

TABLE 3-XVI  
CONDENSED "1" STATE LISTS WITH DO 436 ENERGIZED  
AND PIN6A4J10S FAILED

NORMAL	PIN6A4J10S FAILED
CØIL5A7K440J32PPSJ	CØIL5A7K440J32PPSJ
CØIL5A7K447J31PPGG	CØIL5A7K447J31PPGG
CØNT5A7K440J32SMSN	CØNT5A7K440J32SMSN
CØNT5A7K440J32SQSR	CØNT5A7K440J32SQSR
CØNT5A7K447J31JJKK	CØNT5A7K447J31JJKK
327DI97	327DI97
327DI265	327DI265
327DI267	327DI267
327DI307	327DI307
327DI308	327DI308
327DI336	327DI336
327DI338	327DI338
327DI423	327DI423
327DI425	327DI425
327DI427	327DI427
327DI444	327DI1200
327DI1200	327DI1212
327DI1212	327DI1222
327DI1222	327DØ436
327DØ436	LITE308A1DS14G
LITE308A1DS14G	LITE308A1DS35G
LITE308A1DS35G	LITE308A1DS36G
LITE308A1DS36G	LITE388A5DS7W
LITE388A5DS7W	LITE388A5DS14W
LITE388A5DS14W	LITE388A6DS10W
LITE388A6DS10W	LITE400A12DS63W
LITE400A12DS63W	LITE400A12DS79W
LITE400A12DS79W	LITE400A12DS81W
LITE400A12DS81W	LITE400A12DS83W
LITE400A12DS83W	LITE400A12DS114G
LITE400A12DS114G	LITE400A12DS116G
LITE400A12DS116G	LITE400A12DS118G
LITE400A12DS118G	LITE400A12DS120G
LITE400A12DS120G	MAINFUELVLV1ENG1
LITE400A12DS122G	MAINFUELVLV2ENG1
MAINFUELVLV1ENG1	MAINLØXVLVNØ1ENG1
MAINFUELVLV2ENG1	MAINLØXVLVNØ2ENG1
MAINLØXVLVNØ1ENG1	PØSSWMAINFUELVLV1ENG1
MAINLØXVLVNØ2ENG1	SØLENGICØNTVLVSTART
PØSSWMAINFUELVLV1ENG1	
SØLENGICØNTVLVSTART	

# GENERAL DYNAMICS | CONVAIR

TABLE 3-XVII  
CONDENSED "1" STATE LISTS WITH DO 436 ENERGIZED  
AND SOLENG1CONTVLVSTART FAILED

NORMAL	SOLENG1CONTVLVSTART FAILED
CØIL5A7K440J32PPSJ	CØIL5A7K440J32PPSJ
CØIL5A7K447J31PPGG	CØIL5A7K447J31PPGG
CØNT5A7K440J32SMSN	CØNT5A7K440J32SMSN
CØNT5A7K440J32SQSR	CØNT5A7K440J32SQSR
CØNT5A7K447J31JJJK	CØNT5A7K447J31JJJK
327DI97	327DI97
327DI265	327DI264
327DI267	327DI266
327DI307	327DI307
327DI308	327DI308
327DI336	327DI337
327DI338	327DI339
327DI423	327DI423
327DI425	327DI425
327DI427	327DI427
327DI444	327DI444
327DI1200	327DI1200
327DI1212	327DI1212
327DI1222	327DI1222
327DØ436	327DØ436
LITE3Ø8A1DS14G	LITE3Ø8A1DS14G
LITE3Ø8A1DS35G	LITE3Ø8A1DS35G
LITE3Ø8A1DS36G	LITE3Ø8A1DS36G
LITE388A5DS7W	LITE388A5DS7W
LITE388A5DS14W	LITE388A5DS14W
LITE388A6DS1ØW	LITE388A6DS1ØW
LITE4ØØA12DS63W	LITE4ØØA12DS63W
LITE4ØØA12DS79W	LITE4ØØA12DS79W
LITE4ØØA12DS81W	LITE4ØØA12DS81W
LITE4ØØA12DS83W	LITE4ØØA12DS83W
LITE4ØØA12DS114G	LITE4ØØA12DS115W
LITE4ØØA12DS116G	LITE4ØØA12DS117W
LITE4ØØA12DS118G	LITE4ØØA12DS119W
LITE4ØØA12DS12ØG	LITE4ØØA12DS121W
LITE4ØØA12DS122G	LITE4ØØA12DS122G
MAINFUELVLV1ENG1	
MAINFUELVLV2ENG1	
MAINLØXVLVNØ1ENG1	
MAINLØXVLVNØ2ENG1	
PØSSWMAINFUELVLV1ENG1	
SOLENG1CØNTVLVSTART	

# GENERAL DYNAMICS | CONVAIR

TABLE 3-XVIII  
CONDENSED "1" STATE LIST WITH DO 436 ENERGIZED  
AND POSSWMAINFUELVLV1ENG1 FAILED

## NORMAL

CØIL5A7K440J32PPSJ  
 CØIL5A7K447J31PPGG  
 CØNT5A7K440J32SMSN  
 CØNT5A7K440J32SQR  
 CØNT5A7K447J31JJJK  
 327DI97  
 327DI265  
 327DI267  
 327DI307  
 327DI308  
 327DI336  
 327DI338  
 327DI423  
 327DI425  
 327DI427  
 327DI444  
 327DI1200  
 327DI1212  
 327DI1222  
 327DØ436  
 LITE308A1DS14G  
 LITE308A1DS35G  
 LITE308A1DS36G  
 LITE388A5DS7W  
 LITE388A5DS14W  
 LITE388A6DS10W  
 LITE400A12DS63W  
 LITE400A12DS79W  
 LITE400A12DS81W  
 LITE400A12DS83W  
 LITE400A12DS114G  
 LITE400A12DS116G  
 LITE400A12DS118G  
 LITE400A12DS120G  
 LITE400A12DS122G  
 MAINFUELVLV1ENG1  
 MAINFUELVLV2ENG1  
 MAINLØXVLVNØ1ENG1  
 MAINLØXVLVNØ2ENG1  
 POSSWMAINFUELVLV1ENG1  
 SØLENG1CØNTVLVSTART

## POSSWMAINFUELVLV1ENG1 FAILED

CØIL5A7K440J32PPSJ  
 CØIL5A7K447J31PPGG  
 CØNT5A7K440J32SMSN  
 CØNT5A7K440J32SQR  
 CØNT5A7K447J31JJJK  
 327DI97  
 327DI265  
 327DI267  
 327DI307  
 327DI308  
 327DI337  
 327DI338  
 327DI423  
 327DI425  
 327DI427  
 327DI444  
 327DI1200  
 327DI1212  
 327DI1222  
 327DØ436  
 LITE308A1DS14G  
 LITE308A1DS35G  
 LITE308A1DS36G  
 LITE388A5DS7W  
 LITE388A5DS14W  
 LITE388A6DS10W  
 LITE400A12DS63W  
 LITE400A12DS79W  
 LITE400A12DS81W  
 LITE400A12DS83W  
 LITE400A12DS114G  
 LITE400A12DS116G  
 LITE400A12DS119W  
 LITE400A12DS120G  
 LITE400A12DS122G  
 MAINFUELVLV1ENG1  
 MAINFUELVLV2ENG1  
 MAINLØXVLVNØ1ENG1  
 MAINLØXVLVNØ2ENG1  
 SØLENG1CØNTVLVSTART

## 4/APPLICATIONS FOR DISCRETE NETWORK SIMULATION

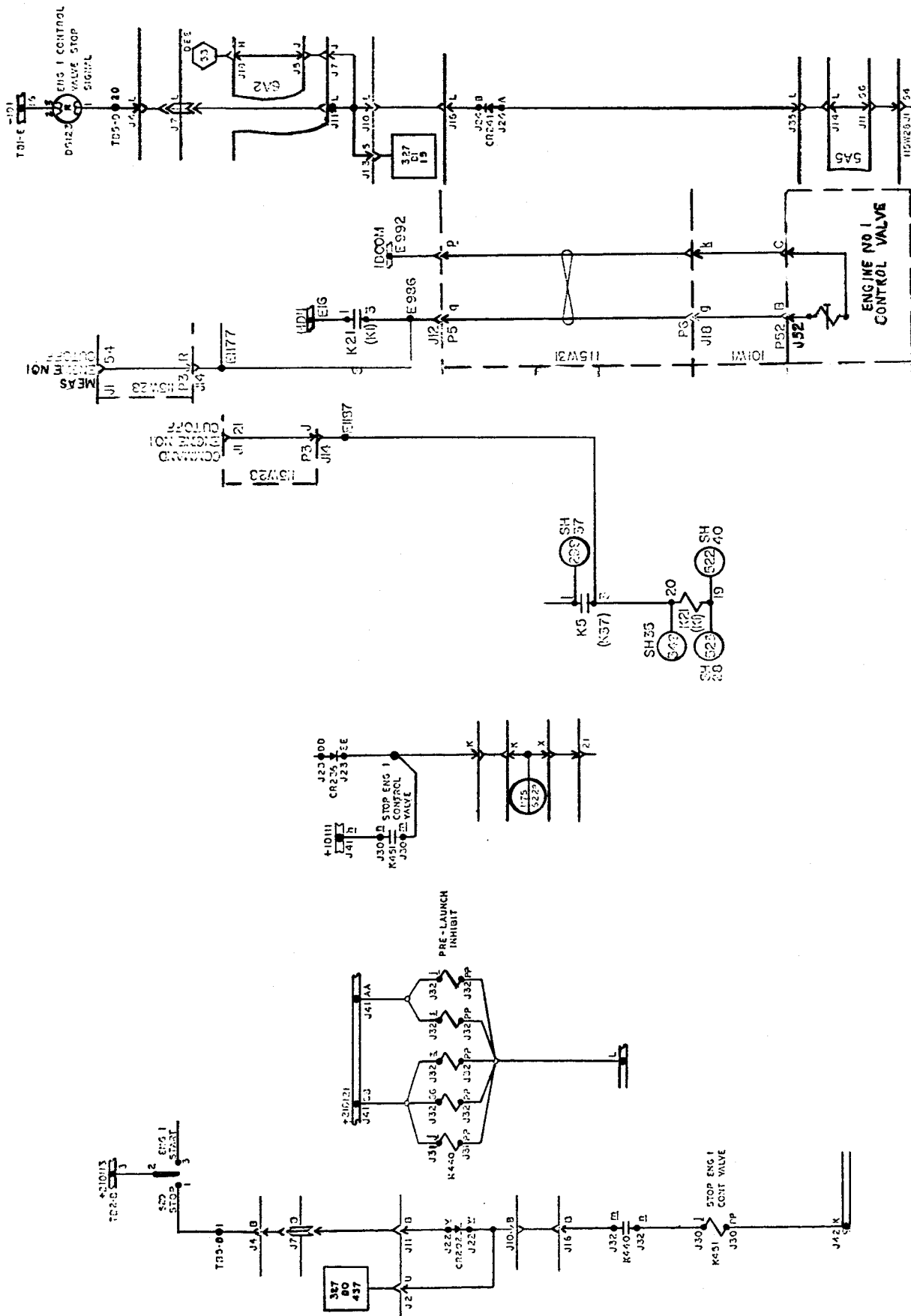
Once the logic model for a hardware system has been built and verified with the Simulation Program as representing the hardware, there are many applications for DNS. Inserting components malfunctions into the simulation and comparing outputs is one of many. DNS applications should be tailored to the objective of the study undertaken. The following examples are possible representative DNS applications for the Saturn Program.

## 4.1 LOGIC DISPLAY

The DNS Programs have the potential capability of drawing out a display in single line format of any circuit of the model. This feature, coupled with the automatic malfunction analysis (AMA), could rapidly provide an exact pictorial display of each circuit in the model that will affect a fault isolated by the AMA. This would provide the necessary documentation to analyze the problem and allow corrective action to be taken without reference to all the necessary schematics.

4.1.1 As an example: If DO 437 (Engine Stop Command) was initiated and a failure was indicated when DI 15 remained in its initial state of "0," research of at least two ESE schematics and one airborne schematic would be required.

The DNS display could produce an uncluttered schematic in two formats. One is in the original format, but with all unnecessary circuitry removed as illustrated in Figure 3-7, and the other is in a simplified format as illustrated in Figure 3-8. The simplified format could be expanded to include pins and plugs as desired. In Figure 3-8 only those pins and plugs are shown that are essential to accomplish circuit checks.



L.H. SIDE TO RH SIDE TO CENTER TO RH SIDE TO L.H. SIDE  
SH. 624 SH. 622 SH. 37 SH. 622

Figure 3-7. Example of composite reproduction of schematics from DNS Programs.

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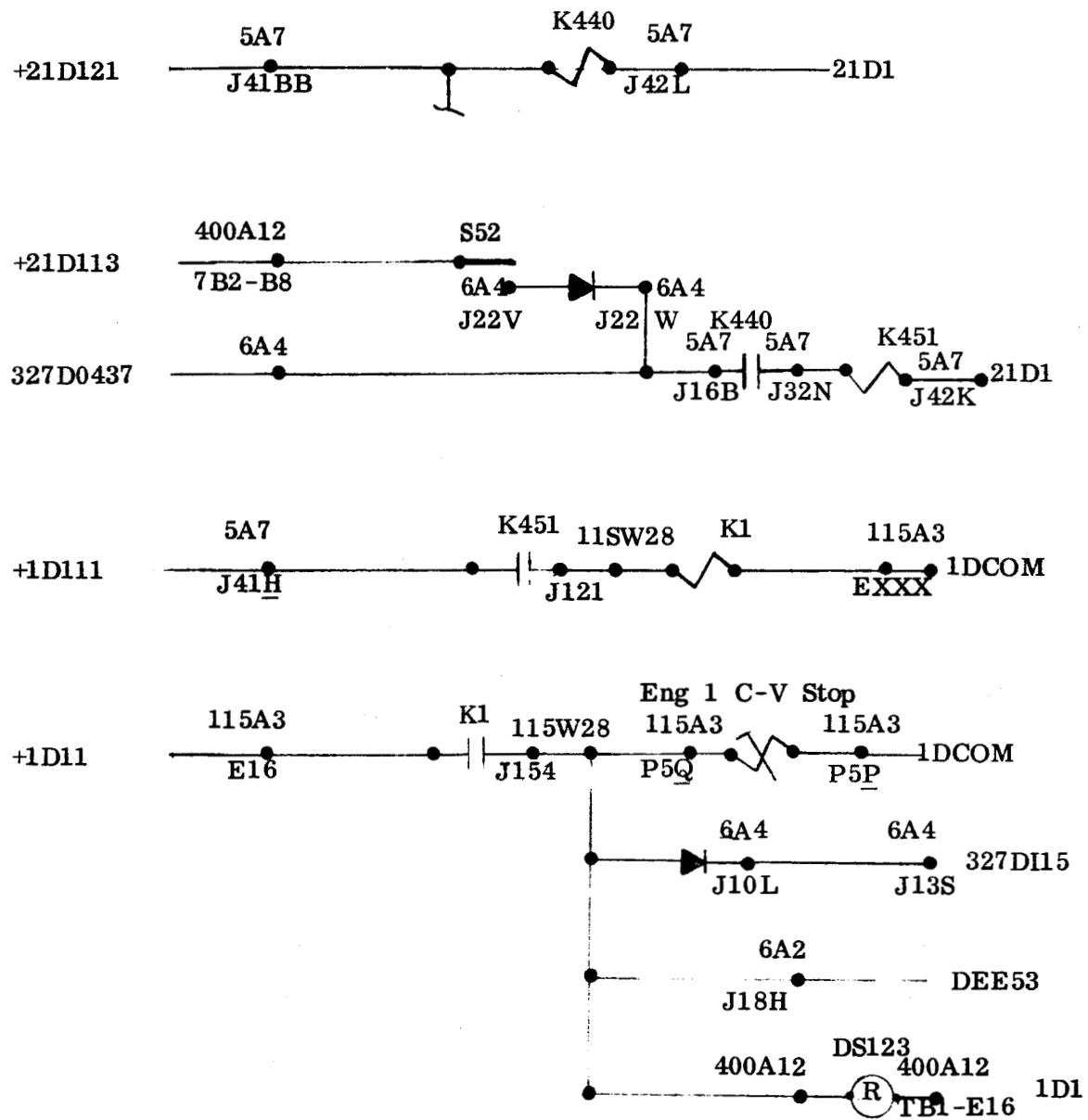


Figure 3-8. Example of simplified schematic from DNS Programs.

#### 4.2 TEST PROCEDURE CHECKING

Test Procedures are normally generated by the design group for a given network. Checkout begins with the sub-system test at the lowest possible level. In many cases the procedure is to activate a single input (Discrete Output, DO) and then check the network operation. When using ATOLL procedures, the anticipated state of the Discrete Inputs (DI's) is loaded into the computer memory and a scan is initiated to check that the DI's do agree with their anticipated state. The listing of the anticipated state of the DI's for a given test is done by the test procedure writer and/or the design engineer. The accuracy of the DI list can be checked, or the information generated by use of the DNS model. One can simulate the results of the checkout procedure by inserting the DO command into the model and listing the status of the DI's on the output. The list of DI's for each DO input can be compared to the checkout procedure prior to the first time the hardware is operated.

#### 4.3 DIGITAL EVENTS EVALUATOR PREDICTION ANALYSIS

The Digital Events Evaluator (DEE-3) records on tape and prints out a history of all the DI's on the stage and in the ESE during any checkout operation. The analysis of the DI activities is a part of the post test analysis. Any unexpected results may indicate faulty operation of a component during the checkout operation. However, during the early part of a program there is no reference data to compare the printout of the DI's on DEE system, too. After running the model in the same mode as the various checkout procedures, the printout of the DI's states in the DNS model can be condensed and tabulated and used as a reference for checking the actual activities of the stage and ESE during checkout. If the number of tests or length of tests are excessive, both the DNS and DEE-3 output can be modified and recorded on tape. The analysis could then be performed by a computer in the checkout complex for future programs.

#### 4.4 AUTOMATED MALFUNCTION ANALYSIS

As discussed in Chapter 3, the insertions of component malfunctions into the DNS model produces data which is then compared to the normal system operation and summary information prepared. Additional studies of this technique have indicated that: (1) very large quantities of data are produced which must be digested and condensed, and, (2) for a large model the number of possible malfunctions and time parameters which must be analyzed makes the required computer time a prohibited factor for a complete analysis. This then requires engineering judgment to select the type of malfunction analysis to be performed.

4.4.1 If malfunction analysis is to be used in support of checkout for launch operations, the analysis must be related to the system status data immediately available.



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For the checkout the status of the Discrete Inputs into the checkout computer gives an accurate representation of the system status. These DI's, in conjunction with the checkout program and program step number, will completely define the status of the stage under test, including the normal state of all the DI signals. Automatic Malfunc-tion Analysis allows one to generate the following information: If during any phase of the operation, a DI indicates an abnormal condition, either "Off" when it should be "On" or "On" when it should be "Off," the analysis will list all single component failures or malfunctions that could cause the DI to be in an abnormal condition. This information can be generated by the additional programs developed to work in conjunc-tion with the DNS Simulation Program. Feasibility studies have been accomplished and the pre-design of this program has already been completed.

4.4.2 As an example: One output option from the Simulation Program generates a complete state list of all variables in the model every time any variable changes state.

CHECKOUT PROGRAM D15-11211  
STEP NO. 021025  
FROM A DNS OUTPUT A HYPOTHETICAL  
NORMAL STATE LIST WOULD BE

DI 963 = 0  
A = 0  
B = 1  
C = 0  
D = 1  
E = 0  
F = 0

The equation for DI 963 is:

$$\begin{aligned} \text{DI963} &= (A * B) + (B * C * D) + E * F \\ (0) &= (0 * 1) + (1 * 0 * 1) + 0 * 0 \end{aligned} \quad (1)$$

If the question is now asked: The normal state of DI963 is "0." What abnormal condition (failure) could cause DI963 to have an abnormal indication, "1?" By inspection it can seem that if "A" or "C" equals "1" it will cause DI963 to become a "1."

This same analysis must then be conducted on "A" and "C" and continued through the complete network. In this way a complete failure mode analysis can be conducted for the total system, based on the monitoring points available during check-out. There are similarities in the checkout procedures and many of the sub-systems

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do not change state during a large portion of the procedures. Therefore, complete malfunction analysis can be made using this technique in a relatively few number of computer hours.

4.4.3 The Automatic Malfunction Analysis and the condensing of the results into a format that can be used during stage checkout can be performed by the IBM 7094 computer by developing additional programs to work with the DNS Programs. In this way, complete malfunction isolation analysis can be made using the DNS model. One way to use the data generated by AMA would be to condense and store all the analysis on magnetic tape. This data would be correlated to the Discrete Input pattern that exists for each test program.

One of the computers available at or near checkout complex could scan the actual status of the DI's in the checkout computer and search the information stored on tape for the DI pattern that matches the actual DI status in the checkout computer. The additional data on the tape would then list or display the possible causes of the indicated malfunction.

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## APPENDICES

- Appendix A    DNS Down Translation and Culling Program listing for S-IC Engine Cutoff System logic model.
- Appendix B    DNS Preprocessor listing of logic equations, and Time Parameters.
- Appendix C    DNS Preprocessor Editor Program listing for logic model.
- Appendix D    DNS Simulation Program listing, Engines Running Condition.
- Appendix E    DNS Simulation Program listing, Engine Cutoff.
- Appendix F    DNS Simulation Program listing, Insertion of Component Malfunctions into S-IC Engine Cutoff System Model.

## NOTE

Due to the specialized content and volume of the Appendices, only two copies were produced.

Copy One has been transmitted to: MSFC-R-QUAL-PS, Attention James H. Newton.

Copy Two will be maintained by: General Dynamics/Convair, Suite 115, Holiday Office Center, Huntsville, Alabama.